ABSTRACT OF THE DISCLOSURE

DELAY LOCKED LOOP

This invention relates to a delay locked loop comprising a line of delay cells (R1, R2, ..., Rn) mounted in series, the delay signal output by the loop being output from the output of one of the delay cells, the input of the delay cells line being connected to a first input of a phase/frequency detector (1), for which a second input is connected to an output from the delay cell.

The loop comprises control means (4) capable of modifying the output from the delay cell connected to the second input of the phase/frequency detector (1), at the rate of a clock signal (H) when stimulated by control information (I).

The invention is particularly applicable to generating and measuring delays and for frequency synthesis in mobile applications.

Figure 2.